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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,179	03/19/2004	Yoshiharu Ogata	81754.0117	7415

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EXAMINER	
PIZARRO CRESPO, MARCOS D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,179	OGATA, YOSHIHARU	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-13 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-13 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-6,9-13 and 17-23* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: 81754.0117
Filing Date: 3/19/2004
Claimed Foreign Priority Date: 3/27/2003 (JP 2003-088829)
Applicant(s): Ogata
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on election filed on 11/7/2005.

Acknowledgment

1. The amendment filed on 11/7/2005, responding to the Office action mailed on 12/5/2003, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-6, 9-13, and 17-23.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the three particles sized to be practically equal to the thickness of the spacer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

6. Claims 6, 9, 10-12, and 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 6, 9 and 10 recite the limitation "the solid material". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, 6, 9-13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over LoBianco (US 6340846) in view of Sauter (US 20020063321).

10. Regarding claim 1, LoBianco shows (see, *e.g.*, fig. 7) all aspects of the instant invention including a semiconductor device **10** comprising:

- ✓ A substrate **20** having a terminal **26** to connect a conductive wire **38**
- ✓ A first semiconductor chip **14** mounted face-up above the substrate **20** and electrically connected to the terminal **26** by the wire **38**
- ✓ A second semiconductor chip **16** mounted above the first chip **14** via an insulating spacer **42**
- ✓ Solid particles **48** contained in the spacer **42** to keep a distance between the chips **14/16** (see, *e.g.*, col.6/ll.7-17)

11. LoBianco fails to specify that the particles have different size. He does, however, teach that each of the solid particles has a diameter approximately equal to the desired final thickness of the spacer (see, *e.g.*, col.6/ll.15-17). Like LoBianco, Sauter (see, *e.g.*, fig. 1) uses solid particles contained in a spacer to keep a distance between two electronic components. Also like LoBianco, he teaches that the size of the particles corresponds to the distance between the components (see, *e.g.*, par.0018/ll.11-18). However, in actual applications, the particles have sizes within a typical plus/minus range around a nominal size, which nominal size corresponds to the distance between the two electronic components (see, *e.g.*, par.0009/ll.10-16). According to Sauter, his

solid particles may be used in LoBianco's insulating spacer to obtain a microelectronic package whereby mechanical distortions resulting from the different thermal expansion coefficients of the chips can be avoided or minimized (see, *e.g.*, par.0009).

12. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to use the solid particles suggested by Sauter, which have different sizes, in LoBianco's insulating spacer to avoid mechanical distortions between the semiconductor chips.

13. Regarding claims 6 and 20, LoBianco (see, *e.g.*, fig. 7, col.6/ll.7-17) and Sauter (see, *e.g.*, par.0018) shows that a size of the solid particles is set corresponding to the distance between the chips.

14. Regarding claim 9, Sauter teaches using the elasticity of the solid particles to reduce the shear effect in the device (see, *e.g.*, par.0015). LoBianco (see, *e.g.*, col.6/ll.40) shows that the elasticity ability of the solid materials is greater than the elasticity of the semiconductor chip since he shows polytetrafluoroethylene (Teflon) particles, which have a higher elasticity than the average semiconductor chip material.

15. Regarding claim 10, LoBianco (see, *e.g.*, fig. 7) and Sauter (see, *e.g.*, fig. 1) shows that the solid particles are globular particles.

16. Regarding claim 11, LoBianco (see, *e.g.*, col.6/ll.15-17) and Sauter (see, *e.g.*, pars. 0009 and 0018) shows that the maximum diameter of the globular particles is practically equal to the thickness of the insulating spacer.

17. Regarding claim 12, Sauter shows that the height of the globular particles is within a range of 1% to 10% the height of the insulating spacer (see, *e.g.*, par.0009).

18. Regarding claim 21, Sauter shows that the radius of the particles in the spacer is between 30 to 150 μm (see, *e.g.*, par.0018/ll.24-25).

19. Regarding claim 22, LoBianco (see, *e.g.*, col.6/ll.15-17) and Sauter (see, *e.g.*, pars. 0009 and 0018) teach that the particles are sized to be practically equal to the thickness of the spacer.

20. Regarding claim 23, LoBianco (see, *e.g.*, fig. 7) and Sauter (see, *e.g.*, fig. 1) shows three of the particles sized to be practically equal to the thickness of the insulating spacer.

21. Regarding claim 2, LoBianco shows (see, *e.g.*, fig. 7) all aspects of the instant invention including a semiconductor device **10** comprising:

- ✓ A substrate **20** having a terminal **26** to connect a conductive wire **38**
- ✓ A first semiconductor chip **14** mounted face-up above the substrate **20** and electrically connected to the terminal **26** by the wire **38**
- ✓ A second semiconductor chip **16** mounted above the first chip **14** via an insulating resin **42**
- ✓ Solid particles **48** contained in the resin **42** to keep a distance between the first and second chips (see, *e.g.*, col.6/ll.7-17)

22. Regarding claim 13, LoBianco shows (see, *e.g.*, fig. 7) all aspects of the instant invention including a semiconductor device **10** comprising:

- ✓ A substrate **20** having a terminal **26** to connect a conductive wire **38**
- ✓ A first electronic part **14** mounted face-up above the substrate **20** and electrically connected to the terminal **26** by the wire **38**

- ✓ A second electronic part **16** mounted above the first electronic part **14** via an insulating spacer **42**
- ✓ Solid particles **48** contained in the insulating spacer **42** to keep a certain distance between the first **14** and the second **16** electronic parts (see, *e.g.*, col.6/ll.7-17)

23. Regarding claims 2 and 13, see also the comments stated above in paragraphs 11 and 12, with respect to claim 1, which are considered repeated here.

24. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over LoBianco/Sauter in view of Fukui (US 6657290).

25. Regarding claims 5 and 17, LoBianco/Sauter shows most aspects of the instant invention (see, *e.g.*, paragraphs 10-23 above), except for an insulating layer formed entirely on a back portion of the second chip. Fukui, on the other hand, teaches that providing said layer to LoBianco's second chip would prevent unwanted contacts to the first chip. In other words, said insulating layer would ensure the insulation of the first chip (see, *e.g.*, Fukui/col.6/ll.25-35).

It would have been obvious at the time of the invention to one of ordinary skill in the art to form an insulating layer on the back of LoBianco/Sauter's second chip, as suggested by Fukui, to ensure the insulation of the first chip.

26. Claims 3, 4, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui in view of Sauter.

27. Regarding claim 3, Fukui shows (see, *e.g.*, fig. 4) most aspects of the instant invention including a semiconductor device comprising:

- ✓ A substrate **7** having a terminal
- ✓ A first semiconductor chip **2** mounted face-up above the substrate **7**
- ✓ A first electrode pad formed on the first chip **2**
- ✓ A first conductive wire **4** electrically connecting the first pad and the terminal
- ✓ A second semiconductor chip **1** mounted above the first chip **2**
- ✓ A second electrode pad formed on the second chip **2**
- ✓ A second conductive wire **3** connecting the second pad and the terminal
- ✓ An insulating resin **6** formed between the first **2** and the second **1** chips wrapping the first wire **4** above the first chip **2**
- ✓ Molding resin **15** to mold the first **2** and second **1** chips

28. Fukui, however, fails to show using solid particles having different sizes to keep a distance between the first and the second chips. Sauter (see, *e.g.*, fig. 1), on the other hand, teaches using solid particles contained in a spacer, similar to Fukui, to keep a distance between two electronic components. He also teaches that the size of the particles corresponds to the distance between the components (see, *e.g.*, pars. 0009 and 0018). However, in actual applications, the particles have different sizes fluctuating within a typical plus/minus range around a nominal size, which nominal size corresponds to the distance between the two electronic components. According to Sauter, his solid particles may be used in Fukui's insulating spacer to obtain a microelectronic package whereby mechanical distortions resulting from the different thermal expansion coefficients of the chips can be avoided or minimized (see, *e.g.*, par.0009).

29. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to use Sauter's solid particles having different sizes in Fukui's insulating spacer to avoid mechanical distortions between the semiconductor chips.

30. Regarding claims 18 and 19, Fukui shows (see, *e.g.*, fig. 4) an insulating layer **5** formed entirely on a back portion of the second chip **1**.

31. Regarding claim 4, Fukui shows (see, *e.g.*, fig. 4) a semiconductor device comprising:

- ✓ A substrate **7** having a terminal
- ✓ A first semiconductor chip **2** mounted face-up above the substrate **7**
- ✓ A first electronic pad formed on the first chip **2**
- ✓ A first conductive wire **4** electrically connecting the first pad and the terminal
- ✓ A second semiconductor chip **1** mounted above the first chip **2**
- ✓ A second electrode pad formed on the second semiconductor chip **1**
- ✓ A second conductive wire **3** electrically connecting the second pad and the terminal
- ✓ An insulating resin **6** mounted between the first **2** and second **1** chips and being at least under the second pad

32. Regarding claim 4, see also the comments stated above in paragraphs 28 and 29, with respect to claim 3, which are considered repeated here.

Response to Arguments

33. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

36. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through

Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

38. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

39. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/777	12/12/2005
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	12/12/2005

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